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Low Power Coding Approach Using of Lagger Algorithm in VLSI Design

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ABSTRACT

The low power has emerged as a principle design requirement in today's electronics industry. The need for low power consumption has become important consideration as performance & area. Even several methods exists, still there requires enhancement for optimization of power consumption in VLSI circuits. There were several approaches in circuit level, but a very few approaches made at system level, such as bus transition power consumption. A large amount of power gets dissipated under the transition of bit sequence from '0' to '1' or '1' to '0' transitions. These powers could be saved if these transitions could be minimized. The power optimization approach in bus transitions using Hamming-coding scheme called 'Lagger algorithm' for transition power reduction in VLSI design is to be developed. As to minimize the transition, the code bit streams are shuffled before transmission using an Encoder unit and bit streams are regenerated using a decoder algorithm by bus shuffling scheme. The proposed work is to be developed on VHDL definition using active HDL tool for its functional simulation and to be synthesized on Xilinx ISE for synthesis and FPGA editor for its practical realization.

Keywords— power optimization, bit transition, lagger algorithm, hamming code, bus shuffling, bit streams.

I.INTRODUCTION

The integration of devices in System On Chip (SOC) the issue of power consumption is increasing. There is a need to develop simpler and efficient low power coding scheme, which can reduce the power consumption at routing level and logical level. Though various techniques were developed to minimize the power consumption in logical devices the other power consumption approaches is also needed to be improved. In this work a focus is given towards minimization of power consumption in data transition time. For the evaluation of the developed approach the coding approach is integrated with an error coding approach to evaluate the minimization of power consumption in transition. The remainder of this paper is organized as follows. In Section II, presents the error coding technique used in the current low power coding approach.

In Section III, the approach of transition minimization is outlined. In Section IV, presents the digital modeling of the suggested approach in modular modeling. In Section V outlines the obtained simulation results obtained for the developed architecture and the timing simulation performed to verify the effectiveness of the proposed approach. Finally, in Section VI, some conclusions are drawn for the presentation of the suggested work.

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II. ERROR CODING TECHNIQUE

Let assume E be the maximum number of error bits that the code can correct and D be the maximum number of error bits that it can detect, and in one error combination that strikes the system let ee, em, and ec be the number of errors in encoder, Digital word, and corrector. This fault secure detector can verify the correctness of the encoder and corrector operation. In any digital system the information bits are fed into the encoder to encode the information.

Vector and the fault secure detector of the encoder verify the validity of the encoded vector. If the detector detects any error, the encoding operation must be redone to generate the correct codeword. Transient errors accumulate in the Digital words over time. In order to avoid accumulation of too many errors in the Digital words that surpasses the code correction capability, the system has to perform Digital scrubbing. Digital scrubbing is periodically reading Digital words from the device, correcting any potential errors and writing them back into the device

.

III. TRANSITION POWER OPTIMIZATION USING SWITCH LOGIC

Buses have been used as an efficient communication link among functional modules in very large scale integration (VLSI) systems. Whereas the size of functional modules decreases with the development of semiconductor technology, the size of VLSI chips increases, and so does the number of functional modules on a chip. Increasing communication requirements among the modules demand more complicated and more efficient buses.

IV.SWITCHING POWER DISSIPATION

This is due to the charging and discharging of capacitive loads during logic changes. The dominant source of power dissipation is thus the charging and discharging of the node capacitances also referred to as the dynamic power dissipation.

The dynamic power dissipation and is given by:

$$P = 0.5\ C\ V_{dd}^2\ E(SW) f_{clk}$$

where C is the physical capacitance of the circuit, Vdd is the supply voltage, E(SW) referred as the switching activity is the average number of transitions in the circuit per 1/fclk is the clock frequency.

A coding scheme called sequence-switch coding (SSC) is developed to reduce the transition power consumption in this work. It is different from previous transition-reduction coding schemes in that it is aimed at applications with the stream-type data transfer pattern.SSC reduces the number of bus transitions by rearranging the transmission sequence of data. An algorithm called switch algorithm is presented to show the feasibility of SSC. This algorithm reduces around 10% of bus transitions in transmission of the benchmark files. For the brevity of description, let us define some terms and notations first. A switched sequence is defined as the sequence of words transmitted according to an SSC algorithm. Let us express the hamming distance between a word, W and a bus, B, as H(W;B).

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The waveforms of eight-bit bus for the eight data are transmitted by the (a) original order and (b) a different order. So far, most of the previous transition-reduction coding schemes have been developed for the granulated data, therefore, they have not considered the sequence of data as an important factor.

SSC is the first general-purpose coding scheme that employs the sequence of data in reducing the number of bus transitions. SSC needs no prior information on data to be sent, and it can be applied to any application that transmits more than two data sequentially for most operations.

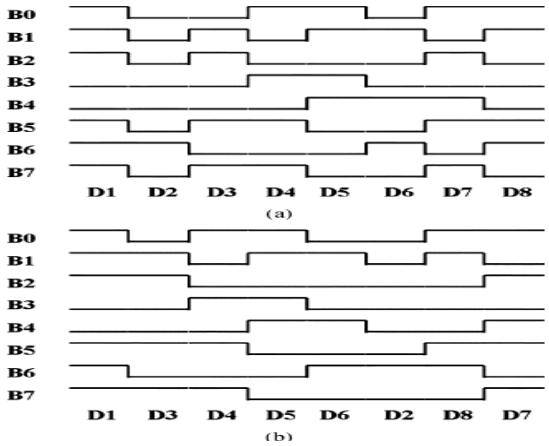

Figure 1:Shows Illustration of the effect of transmission sequence on bus transitions (a) original order (b)Different order

Let us assume that there are 8data to be sent via a bus figure 4.1(a) is the wave form of the bus ,when these are transmitted without any modifications. If the data is sent with a different order example D1-D3-D4-D5-D6-D2-D8-D7,the wave from

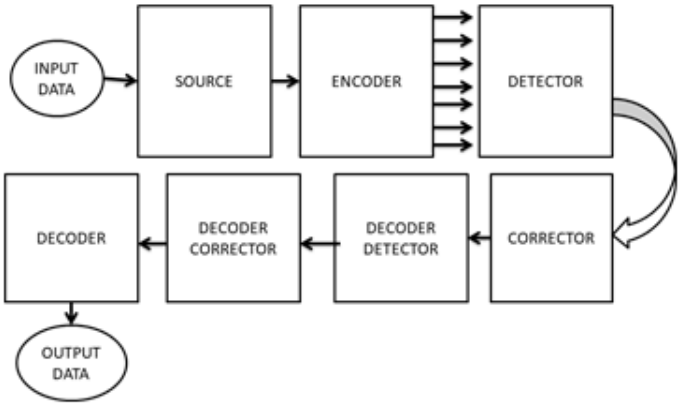

Figure 2: Shows illustrates the operational block diagram for the bus transition minimization using open switch Algorithm

is changed as in figure in 4.1(b).the number of transitions with the new order is 23 compared to 32 with the original order. about 28 percent of bus changing only the transmission order reduces transitions .SSC ,which is based on this observation, is a method intended to reduce the power consumption of busses by changing only the data segment

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V. DESIGN IMPLEMENTATION

A. Bus Transition Optimization Technique

For the optimization of power consumption during data transition a transition optimization for encoding and decoding architecture is developed. Figure 1 illustrates the operational block diagram for the bus transition minimization using open switch Algorithm. The original information bits are passed to the encoding unit, after providing the error coding as explained in previous sections. These information bits are then coded for low transition logic to reduce the power consumption using the suggested switching logic approach as suggested above.

The encoder unit consists of a comparator units and a counter unit for the generation of data stream during coding phase and shown in figure 2.The coding system reads the original data stream and code to generate equivalent coded streams passed as source data to the encoding unit. The source data in binary format is passed to the encoding unit in parallel format and are encoded using Hamming code distance for transition minimizations.

The transition minimization is carried with a parity code and is passed to the decoder for power consumption minimization. The internal functional units for the operation of the suggested architecture is as explained below.

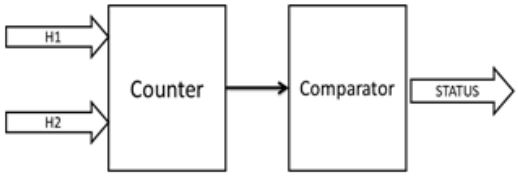

Figure 3: Shows illustrates the comparator units for the operation of bus transition selection using hamming code.

The hamming code comparator unit takes the three input data Din ,Bus and Switch bus for the calculation of hamming distance for Switch and input data with data bus shown in figure 3.

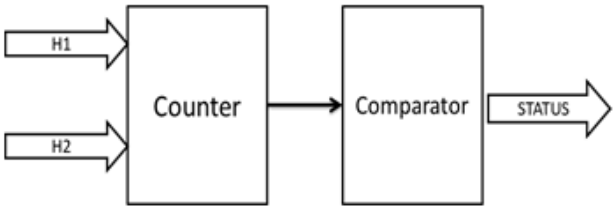

Figure 4: Shows illustrates the code comparator unit.

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The decoder units with storage operation takes the hamming count and generates a count value based on the hamming distance passed the comparison is made and if the hamming distance is observed to be greater than the second value then status signal s=0 is generated or else a '1 'is generated and shown in figure 4.4 ,the decoding operation of the designed system and the probable storage operation for the decoding operation for the decoding operation storing the segregated information for s='1' in digital location(mem1) and s='0' for digital location(mem2).Based on the digital location filled the data is segregated as block1 or block2 information.

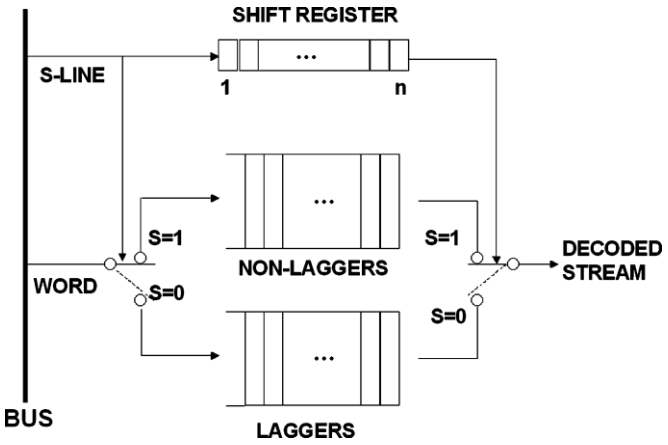

Figure 5: Shows illustrates the Decoder unit with storage Operation

VI. ALGORITHM FOR TRANSITION MINIMISATION

STEPS AS FOLLOWS:

1.For the input data, the data sequence is rearranged to reduce the number of transitions that is hamming distance .The hamming distance means the number of transitions from '1' to '0' or ' 0' to '1'.

2. If the hamming distance reduced then it will reduce the dynamic power consumption. The algorithm for less number of transitions is as follows.

a. The data is rearranged to reduce the number of transitions.
b. The hamming distance for each line is calculated
c. For the entire data the total number of transition is calculated.

VII. RESULT

For the evaluation of the suggested approach an simulation is carried out in active HDL tool and synthesized using xilinx ISE tool. The obtained simulation results are as shown below,

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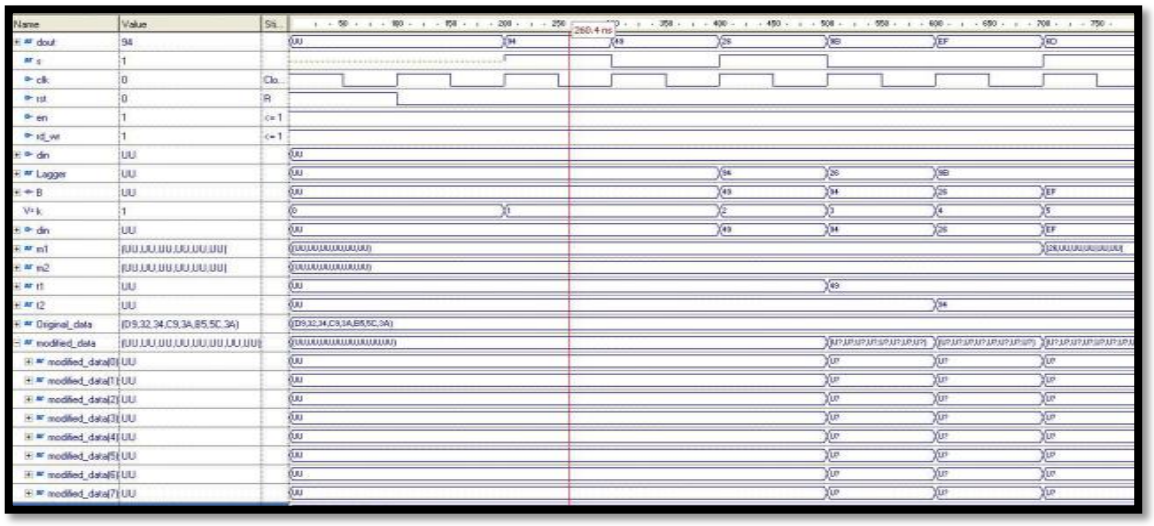
A. TIMING SIMULATION OBSERVATION:

The obtained simulation observation on performing write operation is as illustrated below,



(a)

```
Power summary:                                I(mA)      P(mW)
---------------------------------------------------------------
Total estimated power consumption:                          83
                                              ---
                                Vccint 1.20V:       26        31
                                Vccaux 2.50V:       18        45
                                Vcco25 2.50V:        3         7
                                              ---
                                     Clocks:        0         0
                                     Inputs:        0         0
                                      Logic:        0         0
                                    Outputs:
                                       Vcco25       1         2
                                    Signals:        0         0
                                              ---
                          Quiescent Vccint  1.20V:       26        31
                          Quiescent Vccaux  2.50V:       18        45
                          Quiescent Vcco25  2.50V:        2         5
```

(b)

Figure 6: Shows (a)The simulation result for the developed routing power transition minimization (b) synthesis report

The obtained simulation result for the encoding system is as shown above. The error-coded information's are passed to the encoder unit where a switching scheme is developed for the minimization of transitions to reduce the transition power consumption.

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The modified data passed to the decoder after switch logic transition is shown in figure 6(a) above. It could be observed that the simulation result obtained after the decoding of received modified information is same as the original coded information. This illustrates the accuracy of the developed switch decoder logic after data bit switching. It illustrates the number of data transition seen for the given data which is observed to be reduced from 94 transitions to 49 transitions in the developed approach.

Once the decoded information is retrieved accurately the error decoding system is processed to retrieve the original information back based on the developed error decoding logic. The simulation clearly illustrates that the obtained data stream after the decoding logic is exactly the same as the original data sets. Synthesis Report is shown in figure 6(b)

VIII. CONCLUSION

This work is focused towards the development of minimization of routing transition in digital circuitry. The developed approach is designed for power minimization for a coding system following error-coding algorithm. The operation of error coding is achieved via syndrome encoder and decoder approach and the coded information is evaluated for accuracy using the decoding logic developed. The approach of logical transition for the coded data is developed using open switch logic scheme. Where the coded data stream is passed is switched in an order to minimize transition based the code bit distance.

The developed system is observed to be accurate and provides about 50% lower transition to the original data transfer. The encoding and decoding approach for the developed system is tested for different data word bits and observed to be accurately recovering for up to half the data bit transition. The process of encoding and decoding operation is developed on VHDL.

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